Listing of the Claims:

A clean version of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121(c)(3). This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A capacitor comprising:

a first level of at least four electrically conductive parallel lines extending in a first direction and lying in a first plane;

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at least a second level of at least four electrically conductive parallel lines extending in the first direction and lying in a second plane above the first plane, each of the second level lines being disposed over a respective one of the first level lines, such that the lines of the first and second levels are arranged in a series of at least four coplanar line pairs, each line pair comprising one of the first level lines and a respective one of the second level lines;

a dielectric layer disposed between the first and second levels of conductive lines;

a plurality of vias arranged in a plurality of groups, each group corresponding uniquely to one of the coplanar line pairs and each group including at least two vias connecting the first level line and the second level line of the corresponding line pair, thereby forming an array of at least four parallel capacitor plates; and

electrically opposing nodes forming the terminals of the capacitor, the array of parallel capacitor plates electrically connected to the opposing nodes in an alternating manner so that the plates have alternating electrical polarities.

2. (Original) The capacitor of claim 1, wherein the conductive lines comprise metal.

3. (Original) The capacitor of claim 1, wherein the conductive lines comprise polysilicon.

4. (Original) The capacitor of claim 1, wherein the dielectric layer comprises silicon dioxide.

5. (Previously Presented) The capacitor of claim 1, further comprising:

at least a third level of electrically conductive parallel lines extending in the first direction and lying in a third plane above the first and second planes such that each of the third level lines is coplanar with a respective one of said line pairs; and

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a second dielectric layer disposed between the second and third levels of conductive lines,

so that the third level of lines vertically extends the array of at least four parallel capacitor plates.

6. (Previously Presented) The capacitor of claim 1, wherein the first and the at least second multiple levels of electrically conductive parallel lines comprise a plurality of electrically conductive parallel lines arranged in vertical plates, and the dielectric layer comprises a plurality of dielectric layers, each of the layers disposed between opposing levels of conductive lines.

7. (Original) The capacitor of claim 1, wherein the capacitor is constructed over a substrate.

8. (Original) The capacitor of claim 7, wherein the substrate is made from a semiconductor material.

9. (Original) The capacitor of claim 1, wherein the capacitor comprises a sub-micron MOS structure.

10. (Original) The capacitor of claim 1, wherein the capacitor comprises a sub-micron CMOS structure.

11. (Original) The capacitor of claim 1, wherein the capacitor comprises a sub-micron structure.

12. (Previously Presented) The capacitor of claim 1, wherein each respective plurality of vias of the at least four line pairs of the at least four parallel capacitor plates is arranged opposite a next said respective plurality of vias, with identical spacing of vias in each plurality of vias.

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13. (Currently amended) A capacitor comprising:

a first level of at least four electrically conductive parallel lines extending in a first direction above a substrate;

at least a second level of at least four electrically conductive parallel lines extending in the first direction and lying above the first level, each of the second level lines being disposed over a corresponding one of the first level lines, such that the lines of the first and second levels are arranged in a series of at least four line pairs, each line pair comprising one of the first level lines and the corresponding one of the second level lines disposed thereover;

a dielectric layer disposed between the first and second levels of conductive lines;

a plurality of groups of vias, each group corresponding to one of the line pairs and each group including a plurality of vias directly connecting the first level line and the second level line of the corresponding line pair, thereby forming an array of at least four parallel capacitor plates; and

electrically opposing nodes forming the terminals of the capacitor, the array of parallel capacitor plates electrically connected to the opposing nodes in an alternating manner so that the plates have alternating electrical polarities.

14. (Previously Presented) The capacitor of claim 13, further comprising:

at least a third level of electrically conductive parallel lines extending in the first direction and lying above the first and second levels such that each of the third level lines is disposed over a corresponding one of said line pairs; and

a second dielectric layer disposed between the second and third levels of conductive lines,

wherein the third level of lines vertically extends the array of at least four parallel capacitor plates.

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15. (Previously Presented) The capacitor of claim 13, wherein the vias in each group are identically spaced apart.

16. (Previously Presented) The capacitor of claim 13, wherein each group includes four vias.

17. (Previously Presented) The capacitor of claim 13, wherein the each group includes:

a first via directly connecting the first level line and the second level line of the corresponding line pair at respective first ends of the first and second level lines; and

a second via directly connecting the first level line and the second level line of the corresponding line pair at respective second ends of the first and second level lines,

wherein the second ends are opposite the first ends along the first direction.

18. (Previously Presented) A capacitor comprising:

a first level of at least four electrically conductive parallel lines extending in a first direction;

at least a second level of at least four electrically conductive parallel lines extending in the first direction and lying above the first level, each of the second level lines being disposed over a corresponding one of the first level lines, such that the lines of the first and second levels are arranged in a series of at least four line pairs,

each line pair comprising one of the first level lines and the corresponding one of the second level lines disposed thereover;

a dielectric layer disposed between the first and second levels of conductive lines;

a plurality of groups of vias, each group including a plurality of vias extending directly between the first level line and the second level line of a line pair, thereby forming an array of at least four parallel capacitor plates; and

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electrically opposing nodes forming the terminals of the capacitor, the array of parallel capacitor plates electrically connected to the opposing nodes in an alternating manner so that the plates have alternating electrical polarities.

19. (Previously Presented) The capacitor of claim 18, further comprising:

at least a third level of electrically conductive parallel lines extending in the first direction and lying above the first and second levels such that each of the third level lines is disposed over a corresponding one of said line pairs; and

a second dielectric layer disposed between the second and third levels of conductive lines,

wherein the third level of lines vertically extends the array of at least four parallel capacitor plates.

20. (Previously Presented) The capacitor of claim 17, wherein each group includes four vias.